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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,981	10/20/2003	Beom-jun Jin	5649-1135	8976

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,981	JIN, BEOM-JUN	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/03, 10/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6 and 7 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the conductive plug" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

In re claim 7, the limitation, "wherein the first spacer does not contact the spaced isolated from the contact pad" is vague and indefinite, not accurately setting forth a clear structure.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 6, 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yokoyama (U.S. Patent No. 6,703,715 B2).

In re claim 1, Yokoyama (e.g., Figs. 2C, 3B, 5) discloses an integrated circuit device, comprising:

a conductive contact (32) in a hole in an interlevel dielectric layer,

a first spacer (40/26) having a first dielectric constant on a side wall of the conductive contact; and

a second spacer (38/28) having a second dielectric constant that is less than the first dielectric constant located between the first spacer and the side wall of the conductive contact (column 7, lines 6 – 9).

In re claim 2, Yokoyama discloses the device of claim 1, wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide[1].

In re claim 3, Yokoyama discloses the device of claim 1, wherein the thickness of the first spacer (40/26) is in a range of 1nm to 30nm (column 7, lines 60 – 64).

In re claim 4, Yokoyama discloses the device of claim 1, wherein the thickness of the second spacer (38/28) is in a range between 1nm to 20nm (column 7, lines 60 – 61).

In re claim 5, Yokoyama discloses the device of claim 1, further comprising:

a conductive line (14) in the interlevel dielectric layer adjacent the first spacer opposite the conductive contact.

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[1] Interpreting the claim broadly, silicon oxynitride (SiON) is comprised of silicon oxide.

In re claim 6, as best understood, Yokoyama discloses the device of claim 1, further comprising:

a contact pad (20a) in a substrate, wherein the conductive plug/contact (32) contacts the contact pad.

In re claim 8, Yokoyama (e.g., Figs. 2C, 3B, 5) disclose an integrated circuit device, comprising:

a substrate (10);

a first interlevel dielectric layer (34b) which is formed on the substrate, wherein contact holes are formed in the first interlevel dielectric layer;

first contact spacers (40/26) which are formed along the side walls of the first interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers (38/28) which are formed of silicon nitride and formed on the first spacer; and

contact plugs (32) which are formed between the second contract spacers.

In re claim 9, Yokoyama discloses the device of claim 8, wherein between the substrate and the first interlevel dielectric layer, further comprising:

a second interlevel dielectric (34a) which is formed on the substrate; and

contact pads (36) which are formed in the second interlevel dielectric layer and electrically connected to the contact plugs.

Claims 1 – 4, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Gris et al. (U.S. Patent No. 6,506,655 B1).

In re claim 1, Gris (e.g., Fig. 2F) discloses an integrated circuit device, comprising:

a conductive contact (20) in a hole in an interlevel dielectric layer,

a first spacer (18) having a first dielectric constant on a side wall of the conductive contact; and

a second spacer (16) having a second dielectric constant that is less than the first dielectric constant located between the first spacer and the side wall of the conductive contact (column 7, lines 6 – 9).

In re claim 2, Gris discloses the device of claim 1, wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide.

In re claim 3, Gris discloses the device of claim 1, wherein the thickness of the first spacer (18) is in a range of 1nm to 30nm (column 4, lines 32 – 34).

In re claim 4, Gris discloses the device of claim 1, wherein the thickness of the second spacer (16) is in a range between 1nm to 20nm (column 4, lines 21 – 25).

In re claim 6, as best understood, Gris discloses the device of claim 1, further comprising a contact pad (17) in a substrate, wherein the conductive plug/contact (20) contacts the contact pad.

In re claim 7, as best understood, Gris discloses the device of claim 6, wherein the second spacer (16) extends along the sidewall to contact the contact pad; and

wherein the first spacer does not contact the contact pad.

Claims 1 – 3, 6, and 8 – 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, Park et al. (e.g., Fig. 7) discloses an integrated circuit device, comprising:

a conductive contact (38) in a hole in an interlevel dielectric layer (26a),

a first spacer (24) having a first dielectric constant on a side wall of the conductive contact; and

a second spacer (34) having a second dielectric constant that is less than the first dielectric constant located between the first spacer and the side wall of the conductive contact.

In re claim 2, Park et al. discloses the device of claim 1, wherein the first spacer comprises silicon nitride and the second spacer comprises silicon oxide.

In re claim 3, Park et al. discloses the device of claim 1, wherein the thickness of the first spacer (24) is in a range of 10 to 300 angstroms (column 5, lines 27 – 30).

In re claim 6, as best understood, Park et al. discloses the device of claim 1, further comprising a contact pad (10a) in a substrate, wherein the conductive plug/contact (38) contacts the contact pad.

In re claim 8, Park et al. (e.g., Fig. 7) disclose an integrated circuit device, comprising:

a substrate (1);

a first interlevel dielectric layer (26a) which is formed on the substrate, wherein contact holes are formed in the first interlevel dielectric layer;

first contact spacers (34) which are formed along the side walls of the first interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers (36) which are formed of silicon nitride and formed on the first spacer; and

contact plugs (38) which are formed between the second contract spacers.

In re claim 9, Park et al. discloses the device of claim 8, wherein between the substrate and the first interlevel dielectric layer, further comprising:

a second interlevel dielectric (8) which is formed on the substrate; and

contact pads (10a) which are formed in the second interlevel dielectric layer and electrically connected to the contact plugs.

In re claim 10, Park et al. (e.g., Fig. 7) discloses an integrated circuit device, comprising:

an integrated circuit substrate (1) in which source/drain regions (6s') are formed;

a first interlevel dielectric layer (12a) which is formed on the integrated circuit substrate;

gate line patterns (22) which are formed in the first interlevel dielectric layer;

contact pads (10a) which are present between adjacent gate line patterns in the first interlevel dielectric layer and electrically connected to the source/drain regions;

a second interlevel dielectric layer (26a) which is formed on the first interlevel dielectric layer, wherein contact holes, through which the contact pads are exposed, are formed in the second interlevel dielectric layer;

first contact spacers (34) which are formed along the side walls of the second interlevel dielectric layer which is exposed via the contact holes, the first contact spacers being formed of silicon dioxide;

second contact spacers (36) which are formed of silicon nitride and formed on the first contact spacers; and

contact plugs (38) which are present in the contact holes between the second dielectric spacers.

In re claim 11, Park et al. (e.g., Fig. 1) discloses the device of claim 11, wherein the second interlevel dielectric layer further comprises:

bit line contact plugs which are electrically connected to some of the contact pads; and

bit line patterns which are formed on the bit line contact plugs and electrically connected to eh bit line contact plugs;

wherein the other contact pads, which are not electrically connected to the bit line contact plugs, are exposed through the contact holes.

While not shown in the drawings, such disclosure can be found (column 4, lines 14 – 19; column 4, lines 57 – 61; column 5, lines 6 – 19; column 5, lines 20 – 32; etc.)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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